

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1061	(341/58,87,94,95).CCLS.	USPAT	OR	OFF	2007/03/01 10:57
L2	0	(369/47,48).CCLS.	USPAT	OR	OFF	2007/03/01 10:57
L3	693	(360/32).CCLS.	USPAT	OR	OFF	2007/03/01 10:58
L4	750	(386/112,109).CCLS.	USPAT	OR	OFF	2007/03/01 13:47
L5	18	Mats NEAR1 Oberg	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	AND	ON	2007/03/01 12:59
L6	4	Mats NEAR1 Oberg and metric	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	AND	ON	2007/03/01 13:01
L7	2	"6917313".pn.	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	AND	ON	2007/03/01 13:01

## EAST Search History

L8	0	"6917313".pn. and metric	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	AND	ON	2007/03/01 13:02
L9	2	"6917313".pn. and flip	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	AND	ON	2007/03/01 13:02
L10	5	signal buffer track DC flips "zero"	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2007/03/01 13:48
L11	0	signal buffer track DC flips "zero"	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	WITH	ON	2007/03/01 13:48

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L12	0	signal buffer track DC flips "zero" and I1	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2007/03/01 13:48
L13	0	signal buffer track DC flips "zero" and I3	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2007/03/01 13:48
L14	0	signal buffer track DC flips "zero" and I4	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2007/03/01 13:50
L15	7032	bias transistor base dc	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2007/03/01 13:50

## EAST Search History

L16	0	bias transistor base dc and l1	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2007/03/01 13:51
L17	0	bias transistor base dc and l3	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2007/03/01 13:51
L18	0	bias transistor base dc and l4	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2007/03/01 13:52
L19	79	buffer (track\$2 or tracking) DC (flip\$4 or invert\$4)	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2007/03/01 13:52

## EAST Search History

L20	2	buffer (track\$2 or tracking) DC (flip\$4 or invert\$4) and l1	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2007/03/01 13:54
L21	0	buffer (track\$2 or tracking) DC (flip\$4 or invert\$4) and l3	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2007/03/01 13:54
L22	0	buffer (track\$2 or tracking) DC (flip\$4 or invert\$4) and l4	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2007/03/01 13:54



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## 1 [Power minimization in IC design: principles and applications](#)



Massoud Pedram

January 1996 **ACM Transactions on Design Automation of Electro**

Volume 1 Issue 1

**Publisher: ACM Press**
 Full text available: [pdf\(550.02 KB\)](#) Additional Information: [full citation](#), [citations](#), [index](#)

Low power has emerged as a principal theme in today's electronics industry. Low power has caused a major paradigm shift in which power dissipation is a major concern for performance and area. This article presents an in-depth survey of CAD techniques for designing low power digital CMOS circuits and systems and discusses the issues facing designers at architectural, logical, and physical levels of design. Some of the techniques and tool ...

**Keywords:** CMOS circuits, adiabatic circuits, computer-aided design of low power, power dissipation, energy-delay product, gated clocks, layout, low power layout, lower-power design, power analysis and estimation, power management, power management, probabilistic analysis, silicon-on-insulator technology, static CMOS, capacitance, switching activity, symbolic simulation, synthesis, system simulation

## 2 [Special section: Reasoning about structure, behavior and function](#)



B. Chandrasekaran, Rob Milne




July 1985 **ACM SIGART Bulletin**, Issue 93

**Publisher: ACM Press**Full text available:  [pdf\(5.13 MB\)](#)Additional Information: [full citation, citings](#)

The last several years' of work in the area of knowledge-based systems understanding of the potentials of the current generation of ideas, but r about their limitations and the need for research both in a broader fram directions. The following ideas seem to us to be worthy of note in this c

**3 GPGPU: general purpose computation on graphics hardware**
 David Luebke, Mark Harris, Jens Krüger, Tim Purcell, Naga Govindaraju, I Aaron Lefohn
**August 2004 ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04****Publisher: ACM Press**Full text available:  [pdf\(63.03 MB\)](#)Additional Information: [full citation,](#)

The graphics processor (GPU) on today's commodity video cards has ev powerful and flexible processor. The latest graphics architectures provid bandwidth and computational horsepower, with fully programmable ver units that support vector operations up to full IEEE floating point preci have emerged for graphics hardware, making this computational power GPUs are highly parallel s ...

**4 Computing curricula 2001**
 September 2001 **Journal on Educational Resources in Computing**
**Publisher: ACM Press**Full text available:  [pdf\(613.63 KB\)](#)  [html \(2.78 KB\)](#)Additional Information: [full citation, terms](#)**5 Charles W. Bachman interview: September 25-26, 2004; Tucson, A**
 Thomas Haigh
**January 2006 ACM Oral History interviews****Publisher: ACM Press**Full text available:  [pdf\(761.66 KB\)](#)Additional Information: [full citation,](#)

Charles W. Bachman reviews his career. Born during 1924 in Kansas, B

school in East Lansing, Michigan before joining the Army Anti Aircraft Artillery. He spent two years in the Southwest Pacific Theater, during World War II. In the military, Bachman earned a B.Sc. in Mechanical Engineering in 1948, followed by a M.Sc. in the same discipline, from the University of Pennsylvania. On graduation for Doctor of Philosophy ...


## 6 A design-for-test structure for optimising analogue and mixed signal

A. H. Bratt, A. M. D. Richardson, R. J. A. Harvey, A. P. Dorey

March 1995 **Proceedings of the 1995 European conference on Design for Testability**

**Publisher:** IEEE Computer Society

Full text available:  pdf(964.57

KB) 

Publisher

Site

Additional Information: full citation,

A new Design-for-Test (DfT) structure based on a configurable operational amplifier with a "swap amp" is presented that allows access to embedded analogue blocks with minimal impact on circuit performance and has been evaluated on a custom VLSI Locked Loop (PLL) structure. A test chip containing faulty and fault free structures, with and without DfT modifications, has been fabricated and tested. A scheme based on the swap-amp ...

**Keywords:** DfT modifications, configurable operational amplifier, custom VLSI loop, design for testability, design-for-test structure, diagnostics, embedded integrated circuit testing, mixed analogue-digital integrated circuits, mixed signal operational amplifiers, phase locked loops, swap amp

## 7 Fast detection of communication patterns in distributed executions

Thomas Kunz, Michiel F. H. Seuren

November 1997 **Proceedings of the 1997 conference of the Centre for Collaborative research CASCON '97**

**Publisher:** IBM Press

Full text available:  pdf(4.21

MB)

Additional Information: full citation,





index terms

Understanding distributed applications is a tedious and difficult task. Visual process-time diagrams are often used to obtain a better understanding of an application. The visualization tool we use is Poet, an event tracer developed at Waterloo. However, these diagrams are often very complex and do not provide a desired overview of the application. In our experience, such tools display non-trivial communication patterns ...



**8** Recreational computer graphics: Recreational computer graphics Andrew GlassnerJuly 2006 **ACM SIGGRAPH 2006 Courses SIGGRAPH '06****Publisher:** ACM PressFull text available:  pdf(13.82 MB) Additional Information: [full citation,](#)

Computer graphics isn't just a bunch of algorithms and programs: it's a imagination, and a tool for investigating the world around us. Graphics nature, invent new kinds of patterns and shapes, build up the clarity of experiment with construction tools that would inspire even the most cla painters. Going beyond tools and technique, this course invites attendee computer graphics in new ...

**9** Soviet Computer Technology--1959 March 1960 **Communications of the ACM**, Volume 3 Issue 3**Publisher:** ACM PressFull text available:  pdf(8.23 MB) Additional Information: [full citation,](#)**10** Signal processing at 250 MHz using high-performance FPGA's Brian Von HerzenFebruary 1997 **Proceedings of the 1997 ACM fifth international s programmable gate arrays FPGA '97****Publisher:** ACM PressFull text available:  pdf(1.06 MB) Additional Information: [full citation,](#)  
[terms](#)**11** Robust and low-power clock design: Process variation robust clock Wai-Ching Douglas Lam, Cheng-Kok KohJanuary 2005 **Proceedings of the 2005 conference on Asia South automation ASP-DAC '05****Publisher:** ACM PressFull text available:  pdf(347.53 KB) Additional Information: [full citation,](#)  
[citing](#)

As the minimum feature sizes of VLSI circuits get smaller while the clock effects of process variations become significant. We propose a UST/DME perform simultaneous non-zero clock skew scheduling and clock tree router consideration the effects of process variations on clock skews. Our approach generated clock tree has a high tolerance to process variations while minimizing capacitance of the clock tree, which is ...

## 12 Formal verification in hardware design: a survey



Christoph Kern, Mark R. Greenstreet

April 1999 **ACM Transactions on Design Automation of Electronic Systems**  
Volume 4 Issue 2

**Publisher:** ACM Press

Full text available: [pdf\(411.53 KB\)](#) Additional Information: [full citation, citations, index](#)

In recent years, formal methods have emerged as an alternative approach to the design and correctness of hardware designs, overcoming some of the limitations of traditional techniques such as simulation and testing. There are two main aspects of formal methods in a design process: the formal framework used to specify designs and the verification techniques and tools used to reason about the relationships between designs.

**Keywords:** case studies, formal methods, formal verification, hardware containment, model checking, survey, theorem proving

## 13 A floorplan-based planning methodology for power and clock distribution



Joon-Seo Yim, Seong-Ok Bae, Chong-Min Kyung

June 1999 **Proceedings of the 36th ACM/IEEE conference on Design Automation**

**Publisher:** ACM Press

Full text available: [pdf\(1.19 MB\)](#) Additional Information: [full citation, terms](#)

## 14 Software-controlled fault tolerance



George A. Reis, Jonathan Chang, Neil Vachharajani, Ram Rangan, David I. Dreyer, Mukherjee

December 2005 **ACM Transactions on Architecture and Code Optimization**  
Volume 2 Issue 4

**Publisher:** ACM Press

Full text available: [pdf\(638.90 KB\)](#) Additional Information: [full citation, citations, index](#)

KB)citings, inde

Traditional fault-tolerance techniques typically utilize resources ineffectively to adapt to the changing reliability and performance demands of a system. Software-controlled fault tolerance, a concept allowing designers and users to adapt performance and reliability for each situation. Several software-controlled fault tolerance techniques are then presented: SWIFT, a software-only technique, and hardware/software techniques ...

**Keywords:** Software-controlled fault tolerance, fault detection, reliability

## 15 Performance measurement/content inspection: Design and analysis



from performance, reliability and energy perspective

Jongman Kim, Dongkook Park, Chrysostomos Nicopoulos, N. Vijaykrishnar  
October 2005 **Proceedings of the 2005 symposium on Architectural support for embedded communications systems ANCS '05**

**Publisher:** ACM Press

Full text available: pdf(867.80 KB) Additional Information: full citation, index terms

Network-on-Chip (NoC) architectures employing packet-based communication are increasingly adopted in System-on-Chip (SoC) designs. In addition to providing high performance, the fault tolerance and reliability of these networks is becoming a critical concern in the artifacts of deep sub-micron technologies. Consequently, it is important to have access to fast methods for evaluating the performance, reliability, and energy of a chip network. Towards this ...

**Keywords:** adaptive routing, networks-on-chip, reliability

## 16 The energy complexity of register files



V. Zyuban, P. Kogge

August 1998 **Proceedings of the 1998 international symposium on Low power electronics and design ISLPED '98**

**Publisher:** ACM Press

Full text available: pdf(923.77 KB) Additional Information: full citation, citings, index terms

Register files (RF) represent a substantial portion of the energy budget of a processor and are growing rapidly with the trend towards wider instruction issue. The energy consumption depends greatly on the register file circuitry used. This paper compares various

techniques for their energy efficiencies, as a function of architectural parameters, number of registers and the number of ports. The Port Priority Selection technique ...

## 17 Part 3: adiabatic and energy-recovery circuits: Fast, efficient, recoverable



Visvesh Sathe, Juang-Ying Chueh, Joohee Kim, Conrad H. Ziesler, Suhwar Papaefthymiou

May 2005 **Proceedings of the 2nd conference on Computing frontiers**

**Publisher: ACM Press**

Full text available: [pdf\(543.05 KB\)](#) Additional Information: [full citation](#), [index terms](#)

Recent advances in CMOS VLSI design have taken us to real working charge recovery to operate at substantially lower power dissipation levels than their counterparts. In this paper, we present two such chips that were designed and highlight some of the promising charge-recovery techniques in practice. Since they can be traced back to the early adiabatic circuits, these techniques appear to be a more promising ...

**Keywords:** adiabatic computing, charge-recovery circuits, resonant systems

## 18 Architecture 1: Embedded floating-point units in FPGAs



Michael J. Beauchamp, Scott Hauck, Keith D. Underwood, K. Scott Hemme

February 2006 **Proceedings of the 2006 ACM/SIGDA 14th international conference on Field programmable gate arrays FPGA '06**

**Publisher: ACM Press**

Full text available: [pdf\(831.66 KB\)](#) Additional Information: [full citation](#), [index terms](#)

Due to their generic and highly programmable nature, FPGAs provide a wide range of applications. However, it is this nonspecific nature that hinders their use in scientific applications that require floating-point arithmetic. Even simple operations consume a large amount of computational resources. In this paper, we embed floating-point multiply-add units in an island style FPGA. This results in an average area savings of 55 ...


**Keywords:** FPGA, FPGA architecture, FPU, floating-point

## 19

Time-Varying, Frequency-Domain Modeling and Analysis of Phase-

**Sampling Phase-Frequency Detectors**

Piet Vanassche, Georges Gielen, Willy Sansen

**March 2003 Proceedings of the conference on Design, Automatio  
Volume 1 DATE '03****Publisher: IEEE Computer Society**Full text available:  pdf(147.64KB) Publisher  
SiteAdditional Information: full citation,  
terms

This paper presents a new, frequency-domain based method for modeling locked loop (PLL) small-signal behavior, including time-varying aspects. sampling phase-frequency detectors (PFDs) which compute the phase of the reference signal. Using the harmonic transfer matrix (HTM) formalism continuous-time, linear time-invariant (LTI) approximations are extended to time-varying behavior, arising ...

**20 Memory-efficient and self-stabilizing network RESET (extended abstract)**

Baruch Awerbuch, Rafail Ostrovsky

**August 1994 Proceedings of the thirteenth annual ACM symposium  
distributed computing PODC '94****Publisher: ACM Press**Full text available:  pdf(1.02  
MB)Additional Information: full citation,  
terms

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### 1 Level set and PDE methods for computer graphics

David Breen, Ron Fedkiw, Ken Museth, Stanley Osher, Guillermo Sapiro, R  
August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**

**Publisher:** ACM Press

Full text available: pdf(17.07 MB)

Additional Information: [full citation](#),

Level set methods, an important class of partial differential equation (PDE) for modeling dynamic surfaces implicitly as the level set (iso-surface) of a sampled, scalar field. This course begins with preparatory material that introduces the concept of level set methods and equations to solve problems in computer graphics, geometric modeling and animation. The course will include the structure and behavior of several different types of differential equations. Level set eq ...

### 2 The elements of nature: interactive and realistic techniques

Oliver Deussen, David S. Ebert, Ron Fedkiw, F. Kenton Musgrave, Przemyslaw M. Slomkowski, Roble, Jos Stam, Jerry Tessendorf

August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**

**Publisher:** ACM Press

Full text available: pdf(17.65 MB)

Additional Information: [full citation](#),

This updated course on simulating natural phenomena will cover the latest techniques for simulating most of the elements of nature. The presentation includes production, interactive simulation, and research perspectives on the difficulties of simulating natural phenomena.

modeling, rendering, and animation of natural phenomena. The course  
latest interactive graphics hardware-based simulation techniques and th  
simulation techni ...


### 3 A behavioral signal path modeling methodology for qualitative insight CMOS opamps

Francky Leyn, Walter Daems, Georges Gielen, Willy Sansen

November 1997 **Proceedings of the 1997 IEEE/ACM international  
Computer-aided design ICCAD '97**

**Publisher:** IEEE Computer Society

Full text available:  pdf(159.97

KB) 

Publisher


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Additional Information: full citation,  
citings, inde

This paper describes a new modeling methodology that allows to derive  
signal path models of operational amplifiers. Combined with symbolic si  
provide high qualitative insight in the small-signal functioning of a circu  
path model provides compact interpretable expressions for the poles an  
signal path. These expressions show which design parameters have don  
position of a pole/z ...

**Keywords:** behavioral signal path, incremental modeling, small-signal,  
sequential design space pruning

### 4 Line drawings from 3D models: Line drawings from 3D models

 Szymon Rusinkiewicz, Doug DeCarlo, Adam Finkelstein

July 2005 **ACM SIGGRAPH 2005 Courses SIGGRAPH '05**

**Publisher:** ACM Press

Full text available:  pdf(9.46

MB)

Additional Information: full citation,

### 5 Special section: Reasoning about structure, behavior and function

 B. Chandrasekaran, Rob Milne

July 1985 **ACM SIGART Bulletin**, Issue 93

**Publisher:** ACM Press

Full text available:  pdf(5.13

Additional Information: full citation,

MB)citings

The last several years' of work in the area of knowledge-based systems understanding of the potentials of the current generation of ideas, but r about their limitations and the need for research both in a broader fram directions. The following ideas seem to us to be worthy of note in this c

## **6** Recorded magnetic tape for information interchange (800 CPI, NRZ



S. Gorn

April 1966 **Communications of the ACM**, Volume 9 Issue 4**Publisher:** ACM Press

Full text available: pdf(1.36 MB)

Additional Information: full citation

## **7** Exploiting perception in high-fidelity virtual environments: Exploiting fidelity virtual environments



**Additional presentations from the 24th course are available on**  
Mashhuda Glencross, Alan G. Chalmers, Ming C. Lin, Miguel A. Otaduy, Di  
July 2006 **ACM SIGGRAPH 2006 Courses SIGGRAPH '06**

**Publisher:** ACM Press

Full text available: pdf(5.07 MB) mov (68:6 MIN)

Additional Information: full citation,

The objective of this course is to provide an introduction to the issues th when building high-fidelity 3D engaging shared virtual environments. Th perception guide important development of algorithms and techniques i auditory, and haptic rendering. We aim to show how human perception realism in high fidelity environments within the constraints of available resources. In this course w ...

**Keywords:** collaborative environments, haptics, high-fidelity rendering interaction, multi-user, networked applications, perception, virtual realit


## **8** A control-theoretic approach to adapting VBR compressed video for communications channel

Soung C. Liew, Derek Chi-yin Tse

February 1998 **IEEE/ACM Transactions on Networking (TON)**, Vo



**Publisher:** IEEE Press

Full text available:  pdf(429.79 KB) Additional Information: [full citation](#),


**Keywords:** rate control, traffic adaptation, video compression, video tr control

## 9 Power minimization in IC design: principles and applications

 Massoud Pedram

January 1996 **ACM Transactions on Design Automation of Electro**  
Volume 1 Issue 1

**Publisher:** ACM Press

Full text available:  pdf(550.02 KB) Additional Information: [full citation](#),  
[citations](#), [index](#)

Low power has emerged as a principal theme in today's electronics indu power has caused a major paradigm shift in which power dissipation is performance and area. This article presents an in-depth survey of CAD techniques for designing low power digital CMOS circuits and systems a issues facing designers at architectural, logical, and physical levels of de some of the techniques and tool ...


**Keywords:** CMOS circuits, adiabatic circuits, computer-aided design of dissipation, energy-delay product, gated clocks, layout, low power layou lower-power design, power analysis and estimation, power managemen management, probabilistic analysis, silicon-on-insulator technology, sta capacitance, switching activity, symbolic simulation, synthesis, system (

## 10 Recorded magnetic tape for information interchange (1600 CPI, phe

 C. Kerpelman

November 1970 **Communications of the ACM**, Volume 13 Issue 11

**Publisher:** ACM Press

Full text available:  pdf(1.00 MB) Additional Information: [full citation](#),

This proposed American National Standard has been accepted for public Standards Committee X3, Computers and Information Processing. In or the proposed standard reflect the largest public consensus, X3 authoriz

document to elicit comment and general public reaction, with the under working document is an intermediate result in the standardization process change, modification ...

**Keywords:** information interchange, input-output, instrumentation, magnetic phase encoded recording

## 11 Draft Proposed: American National Standard—Graphical Kernel System



Technical Committee X3H3 - Computer Graphics

February 1984 **ACM SIGGRAPH Computer Graphics**, Volume 18 Issue 1

**Publisher:** ACM Press

Full text available: pdf(16.07 MB)

Additional Information: [full citation](#)

## 12 GPGPU: general purpose computation on graphics hardware



David Luebke, Mark Harris, Jens Krüger, Tim Purcell, Naga Govindaraju, Isaac Aaron Lefohn

August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**

**Publisher:** ACM Press

Full text available: pdf(63.03 MB)

Additional Information: [full citation](#)

The graphics processor (GPU) on today's commodity video cards has evolved into a powerful and flexible processor. The latest graphics architectures provide high bandwidth and computational horsepower, with fully programmable vertex and fragment processing units that support vector operations up to full IEEE floating point precision. These units have emerged for graphics hardware, making this computational power available to a wide range of applications. GPUs are highly parallel structures ...

## 13 System-level power optimization: techniques and tools



Luca Benini, Giovanni de Micheli

April 2000 **ACM Transactions on Design Automation of Electronic Systems**, Volume 5 Issue 2

**Publisher:** ACM Press

Full text available: pdf(385.22 KB)

Additional Information: [full citation](#), [citations](#), [index](#)

This tutorial surveys design methods for energy-efficient system-level design

electronic systems consisting of a hardware platform and software layers  
major constituents of hardware that consume energy, namely computation  
storage units, and we review methods of reducing their energy consumption  
for analyzing the energy cost of software, and methods for energy-efficient  
compilation. This survey ...

#### 14 Seeing, hearing, and touching: putting it all together

 Brian Fisher, Sidney Fels, Karon MacLean, Tamara Munzner, Ronald Rensin  
August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**

**Publisher:** ACM Press

Full text available:  pdf(20.64 MB)

Additional Information: [full citation](#)

#### 15 MPEG-4: an object-based multimedia coding standard supporting m

Atul Puri, Alexandros Eleftheriadis

June 1998 **Mobile Networks and Applications**, Volume 3 Issue 1

**Publisher:** Kluwer Academic Publishers



Full text available:  pdf(747.80 KB) Additional Information: [full citation](#), [citations](#), [index](#)

The ISO MPEG committee, after successful completion of the MPEG-1 and MPEG-2 standards, is currently working on MPEG-4, the third MPEG standard. Originally, MPEG-1 was a standard for coding of limited complexity audio-visual scenes at very low bit rates. In July 1994, its scope was expanded to include coding of scenes as a collection of visual objects and enabling a range of advanced functionalities not supported by MPEG-1. One of the key features of MPEG-4 is the ability to represent individual objects in a scene and to manipulate them independently of each other.

#### 16 Computing curricula 2001

 September 2001 **Journal on Educational Resources in Computing**

**Publisher:** ACM Press

Full text available:  pdf(613.63 KB)  html (2.78 KB)

Additional Information: [full citation](#), [terms](#)

#### 17 Analog macromodeling: Automated nonlinear Macromodelling of our speed digital applications

- ◆ Ning Dong, Jaijeet Roychowdhury  
June 2005 **Proceedings of the 42nd annual conference on Design**  
**Publisher:** ACM Press

Full text available:  [pdf\(1.30 MB\)](#) Additional Information: [full citation](#), [index terms](#)


We present applications of a recently developed automated nonlinear m the important problem of macromodelling high-speed output buffers/dri macromodels of such drivers are essential for fast signal-integrity and t speed digital design. Unlike traditional black-box modelling techniques, nonlinear macromodels of digital drivers *automatically* from SPICE-level naturally capture t ...

**Keywords:** I/O buffer macromodeling, nonlinear macromodeling

- 18** Proceedings of the SIGNUM conference on the programming envirc  
of numerical software

◆ March 1979 **ACM SIGNUM Newsletter**, Volume 14 Issue 1


**Publisher:** ACM Press

Full text available:  [pdf\(5.02 MB\)](#) Additional Information: [full citation](#)

- 19** Network Protocols

◆ Andrew S. Tanenbaum  
December 1981 **ACM Computing Surveys (CSUR)**, Volume 13 Issue

**Publisher:** ACM Press

Full text available:  [pdf\(3.37 MB\)](#) Additional Information: [full citation](#), [terms](#)

- 20** Charles W. Bachman interview: September 25-26, 2004; Tucson, A

◆ Thomas Haigh  
January 2006 **ACM Oral History interviews**

**Publisher:** ACM Press

Full text available:  [pdf\(761.66 KB\)](#) Additional Information: [full citation](#),

Charles W. Bachman reviews his career. Born during 1924 in Kansas, Bachman attended high school in East Lansing, Michigan before joining the Army Anti Aircraft Artillery. He spent two years in the Southwest Pacific Theater, during World War II. After leaving the military, Bachman earned a B.Sc. in Mechanical Engineering in 1948, followed by an M.Sc. in the same discipline, from the University of Pennsylvania. On going to work for Do ...

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